



(11) Publication number : **0 253 631 B1**

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication of patent specification :  
**22.04.92 Bulletin 92/17**

(51) Int. Cl.<sup>5</sup> : **G11C 11/24, G11C 11/401**

(21) Application number : **87306225.1**

(22) Date of filing : **14.07.87**

(54) **Semiconductor memory device.**

(30) Priority : **14.07.86 JP 163849/86**

(43) Date of publication of application :  
**20.01.88 Bulletin 88/03**

(45) Publication of the grant of the patent :  
**22.04.92 Bulletin 92/17**

(84) Designated Contracting States :  
**DE FR GB**

(56) References cited :  
**EP-A- 0 135 036**  
**US-A- 4 507 758**  
**IBM TECHNICAL DISCLOSURE BULLETIN,**  
**vol. 28, no. 10, March 1986, pages 4299-4300,**  
**New York, US; "Two-device nondestructive**  
**read-out cell with stacked metal oxide semi-**  
**conductor devices"**

(56) References cited :  
**PATENT ABSTRACTS OF JAPAN, vol. 7, no.**  
**174 (E-190)[1319], 2nd August 1983; & JP-A-58**  
**80 864 (FUJITSU K.K.) 16-05-1983**  
**IBM TECHNICAL DISCLOSURE BULLETIN,**  
**vol. 27, no. 6, November 1984, pages**  
**3348-3350, New York, US; R.F. PENOYER:**  
**"Integrated JFET/IGFET memory cell"**

(73) Proprietor : **OkI Electric Industry Company,**  
**Limited**  
**7-12, Toranomom 1-chome Minato-ku**  
**Tokyo 105 (JP)**

(72) Inventor : **Sasaki, Masayoshi**  
**OkI Electric Ind. Co. Ltd. 7-12, Toranomom**  
**1-chome**  
**Minato-ku Tokyo 105 (JP)**

(74) Representative : **Boydell, John Christopher et**  
**al**  
**Stevens, Hewlett & Perkins 1 Serjeants' Inn**  
**Fleet Street**  
**London EC4Y 1LL (GB)**

**EP 0 253 631 B1**

Note : Within nine months from the publication of the mention of the grant of the European patent, any person may give notice to the European Patent Office of opposition to the European patent granted. Notice of opposition shall be filed in a written reasoned statement. It shall not be deemed to have been filed until the opposition fee has been paid (Art. 99(1) European patent convention).

conduction or nonconduction of the second MOS transistor.

In an embodiment of the invention, the first MOS transistor, serving as a data writing transistor, a charge storage electrode, and the second MOS transistor, serving as a data reading transistor are provided in stack with each other, so that an amplification function is achieved by use of a smaller area. Moreover, the conductivity types of the data writing transistor and the data reading transistor are opposite to each other, and the gate electrodes of the respective transistors are capacitively coupled with the charge storage electrode, so that writing data and reading data can be controlled by a common word line. Furthermore, an SOI polysilicon transistor can be used as the data reading transistor, and fabrication of the memory device is facilitated.

In order that the invention may be better understood, several embodiments thereof will now be described by way of example only and with reference to the accompanying drawings in which:-

Figure 1 is a cross sectional view showing the memory cell of a prior art DRAM;

Figure 2 is a plan view showing a prior art gain cell;

Figure 3 is a cross sectional view showing the gain cell of Figure 2;

Figure 4 is a circuit diagram showing an equivalent circuit of the gain cell of Figure 2;

Figure 5 is a cross sectional view showing an embodiment of a semiconductor device of the invention;

Figures 6a and 6b are plan views showing, at different levels or layers, the semiconductor device of Figure 5;

Figure 7 is a circuit diagram showing an equivalent circuit showing the semiconductor device of Figure 5;

Figures 8a to 8f show operations of the device of Figure 5;

Figure 9 is a table showing voltage values at different operating states of the device of Figure 5;

Figure 10 is a simplified circuit diagram for analysis of the voltage on the data charge storage electrode;

Figure 11 shows a subthreshold characteristic of a polysilicon transistor according to the invention;

Figure 12 is a circuit diagram showing an equivalent circuit of a second embodiment of the invention;

Figures 13a and 13b are plan views showing, at different levels or layers, the semiconductor device of Figure 12;

Figure 14 is a diagram showing a third embodiment of the semiconductor memory device of the invention;

Figure 15 is a cross sectional view showing the semiconductor memory device of Figure 14;

Figure 16 is a cross sectional view showing a modification of the embodiment of Figures 14 and 15; and

Figure 17 is a cross sectional view showing a modification of the embodiment of Figure 5.

Figure 5 shows a cross section of a gain cell of a semiconductor memory device of a first embodiment of the invention, and Figures 6a and 6b are plan views of the gain cell of Figure 5, as seen at different layers. More particularly, Figure 6a shows a polysilicon transistor and an A1 bit line on the upper layer, while Figure 6b shows layers below the electrodes of the charge storage capacitor. The points denoted by mark A in Figures 6a and 6b are in alignment with each other along the vertical direction so that they should be made to align when Figures 6a and 6b are seen in stack. Figure 7 is an equivalent circuit diagram of the gain cell shown in Figures 5, 6a and 6b.

The gain cell of the embodiment comprises a p-type silicon substrate 21, an element isolation silicon dioxide ( $\text{SiO}_2$ ) film, a data writing transistor Q1 having a source (n-type region) 23, a drain (n-type region) 24 and a gate electrode 25. The writing transistor Q1 is shown to be an n-channel MOSFET. The drain 24 of the writing transistor Q1 is connected to a polysilicon electrode 28, which is opposite to the gate electrode 25 across a thin insulating film 27 to form a capacitor C1 (Figure 7). A layer 36 of polysilicon is provided over the polysilicon electrode 28, being separated by a thin insulating film 32 forming a gate oxide film. The polysilicon layer 36 has regions 31 and 29 doped to be of a p-type and another region 30 doped to be of an n-type. The regions 31, 29 and 30 serve respectively as a source, a drain and a channel of p-channel data reading MOSFET Q2. The polysilicon electrode 28 serves as a gate electrode of the MOSFET Q2. This MOSFET Q2 is formed on an insulator, i.e. it is an SOI (silicon on insulator) transistor. The source 31 of the transistor Q2 is in contact with the source 23 of the transistor Q1 to form a pn junction diode. The source 31 is also connected to an A1 bit line 34. The A1 bit line 34 and the polysilicon layer 36 are separated by an insulating layer 33 and the polysilicon layer 36 and the silicon substrate 21 are separated by an insulating layer 35.

As can be seen from the structure illustrated in Figure 5 and an equivalent circuit illustrated in Figure 7, the polysilicon electrode 28 in Figure 5 corresponds to a node N1 in Figure 7. The capacitance between the polysilicon electrode 28 and the channel 30 forms a capacitor C1, and the capacitance between the polysilicon electrode 28 and the gate electrode 25 forms a capacitor C2. The polysilicon gate electrode 25 also serves as a word line.

The operation of the gain cell of Figures 5 to 7 will be described in detail with reference to Figures 8a to 8f. Figures 8a, 8b and 8c respectively show the states of the cell at the time of writing, maintaining and reading logic "1" data, and Figures 8d, 8e and 8f respectively show the states of the cell at the time of writing, maintaining and reading logic "0" data.

Q2 being turned on and  $V_b$  being negative, thereby forward-biasing a diode formed of the n-type source 23 of the transistor Q1 and the p-type substrate 21.

Incidentally, when  $V_b$  is positive, the diode between the source 31 of the transistor Q2 and the substrate 21 of the transistor Q1 is forward-biased. But the substrate of the transistor Q2 is floating. The current must therefore flow through a pn junction between the drain 29 of the transistor Q2 and the substrate. The drain-substrate diode is however off. Accordingly, no current flows through the source 31 of the transistor Q2 and the substrate even when  $V_b$  is positive.

An SOI transistor is used as the data reading transistor. To form an SOI transistor, a technique for recrystallising polysilicon by laser irradiation is being studied, and this method can be employed for realising the SOI transistor. Other methods can be equally employed. But it should be noted that the invention does not require the characteristic of the SOI transistor to be so good as was required in the prior art gain cell. This is because it is sufficient that there is a certain distinction between on and off during reading. Thus a polysilicon transistor can be used.

Figure 11 shows the subthreshold (drain current versus gate voltage) characteristic of a polysilicon transistor used in the invention. It is assumed that the gate length  $L$  is 10 micrometers, the gate width  $W$  is 112 micrometers, the gate oxide film thickness  $T_{ox}$  is 38nm. The two curves are for drain voltages  $V_d$  of 5V and 0.5V, respectively.

The on/off current ratio is about  $10^4$  and the gradient of the curve in the subthreshold region is about 500mV/dec or less. This characteristic is satisfactory for the cell of the invention.

In the embodiment described, the transistor Q1 is an n-channel MOSFET and the transistor Q2 is a p-channel MOSFET. But alternatively the transistors Q1 and Q2 can be of a p-channel and an n-channel, respectively, with the polarities of the voltages at various terminals or nodes being reversed. Similar operation and results can be obtained by such alteration.

In the embodiment described, the charge storage region is formed of polysilicon surrounded by an  $\text{SiO}_2$  layer and the drain 24 of the transistor Q1 connected thereto. Reduction in the stored charge is dependent on leakage through the  $\text{SiO}_2$  and leakage through the drain-substrate. But these can be easily controlled to be sufficiently small.

The structure of the embodiment is also advantageous in that soft errors due to alpha particles are reduced. Soft errors are caused when electric charges generated in the substrate due to alpha particles flow into the drain region. But in the embodiment, the area of the drain region is small so that flow of the electric charges into the drain region can be made small, and hence soft errors are reduced.

Moreover, if a p<sup>-</sup>/p<sup>+</sup> epitaxial structure is built in the substrate, the resistance to soft error is further improved.

Figure 12 is an equivalent circuit diagram showing a second embodiment of the invention.

Figures 13a and 13b are plan views of the embodiment of Figure 12 at different levels corresponding to Figures 6a and 6b. That is, Figure 13a shows the upper polysilicon transistor and an A1 bit line, while Figure 13b shows the electrode of the charge storage capacitor, and other layers below it. The points with a mark A in Figures 13a and 13b are in alignment with each other. In this embodiment, two separate bit lines are provided, one 41 ( $V_{bw}$ ) for writing and the other 42 ( $V_{br}$ ) for reading. The rest of the structure is similar to that of the first embodiment of Figure 5. Particularly, the members or parts denoted by the same reference as in Figures 5 to 7 have similar functions.

In the embodiment of Figures 12, 13a and 13b, two bit lines are required, but the diode D1 in the first embodiment is eliminated and the need to handle four different values of voltages on the same bit line (as required in the first embodiment) is eliminated. According to this embodiment, there should appear two different values on the writing bit line and two different values on the reading bit lines, so that the peripheral circuits are easier to design.

Figure 14 is an equivalent circuit diagram of a third embodiment of the invention. In this embodiment, a diode D2 is inserted between the drain of the transistor Q1 and the charge storage electrode N1. If, during writing,  $V_w$  is made to be larger than  $V_{bw}$  to forward-bias this diode D2, electric charge is stored on the charge storage electrode. In the first and the second embodiments, when  $V_c$  becomes negative, the diode between the drain of the transistor Q1 and the substrate is forward-biased, and the stored charge is lost. The insertion of the diode D2 prevents such loss of the stored charge. Freedom of design in setting the word line voltage  $V_w$  and the writing voltage  $V_{bw}$  is thereby enlarged.

The diode D2 can be formed if, for example, the polysilicon layer 28 is doped to be of a p-type layer 28A (Figure 15), so that a p-n junction is formed between the polysilicon layer 28A and the n-type drain region 24. As an alternative, a metal electrode 28B (Figure 16) is formed instead of the polysilicon layer 28 (to constitute the charge storage electrode), so that a Schottky junction diode is formed between the metal electrode 28B and the drain 24.

The diode D1 can also be in the form of a Schottky junction diode. This can be implemented by inserting

said control means applies a first potential to the word line to make conductive the first MOS transistor for writing data, applying a first potential to the source of the first MOS transistor, for writing data "1", and applying a second potential to the source of the first MOS transistor for writing data "0";

said control means applies a second potential to the word line to keep the first transistor nonconductive  
5 for maintaining the data stored on the charge storage electrode; and

said control means applies a third potential to the word line for reading data, to change the potential on the charge storage electrode to make the second MOS transistor conductive or nonconductive depending on the data stored on the charge storage electrode, thereby transmitting or not transmitting the potential from the power supply to the source of the second MOS transistor and hence to the bit line connected thereto, the transmission and non-transmission of the potential from the power supply providing different potentials on the bit line connected to the source of the second transistor.  
10

9. A device according to claim 8, wherein the first MOS transistor is an n-channel transistor, and the second MOS transistor is a p-channel transistor, and the third potential as applied to the word line is lower than the second potential as applied to the word line, which in turn is lower than the first potential as applied to the first potential, and the second potential as applied to the source of the first MOS transistor is lower than the first potential as applied to the source of the second MOS transistor.  
15

10. A device according to claim 8, wherein the source of the first MOS transistor and the source of the second MOS transistor is in contact with each other to form a pn junction diode, and the source of the second transistor is connected to the common bit line used both for writing and reading.

11. A device according to claim 8, wherein the source of the first MOS transistor and the source of the second MOS transistor is in contact with each other through a metal layer to form a pn Schottky junction diode between the metal layer and the one of the sources, and the source of the second transistor is connected to the common bit line used both for writing and reading.  
20

12. A device according to claim 8, wherein the channels of the first and the second transistors extend in the direction of the bit lines and the word lines extend in a direction orthogonal to the direction of the bit lines.  
25

13. A device according to any one of the preceding claims comprising a matrix of said memory cells.

## Patentansprüche

30

1. Halbleiterspeichereinrichtung mit einer Speicherzelle, die aufweist:

einen ersten MOS-Transistor (Q1) eines ersten Kanaltyps, der auf einem Halbleitersubstrat ausgebildet ist und der eine Gate-Elektrode, die mit einer Wortleitung verbunden ist, eine Drain und eine Source hat, wobei die Source mit einer Bitleitung (31) verbunden ist;

35

eine Ladungsspeicherelektrode (28), die mit der Drain des ersten Transistors verbunden ist;

eine Halbleiterschicht (29, 30, 31), die über der Ladungsspeicherelektrode ausgebildet ist und von der Ladungsspeicherelektrode durch einen Isolationsfilm getrennt ist;

40

einen zweiten MOS-Transistor (Q2) eines zweiten Kanaltyps, der unterschiedlich zu dem ersten Kanaltyp ist, in der Halbleiterschicht ausgebildet ist und eine Source und eine Drain hat, wobei die Ladungsspeicherelektrode des ersten MOS-Transistors eine Gate-Elektrode des zweiten MOS-Transistors bildet;

wobei die Drain des zweiten Transistors mit einer Spannungsversorgung verbunden ist;

wobei die Source des zweiten Transistors mit einer Bitleitung verbunden ist, die entweder die gleiche wie die erste erwähnte Bitleitung ist oder eine von der ersten erwähnten Bitleitung getrennte ist;

45

wobei die Speichereinrichtung weiterhin aufweist, eine Steuereinrichtung zum Steuern des Schreibens und Lesens von Daten in bzw. von der Speicherzelle;

wobei die Steuereinrichtung Daten schreibt, indem sie das Potential auf der Wortleitung und der Bitleitung, die mit dem ersten MOS-Transistor verbunden ist, steuert, um eine elektrische Ladung entsprechend den Daten auf der mit dem ersten Transistor verbundenen Bitleitung zuzuführen;

50

wobei die Halbleiter-Speichereinrichtung dadurch gekennzeichnet ist, daß die Ladungsspeicherelektrode (28) über der Gate-Elektrode des ersten Transistors ausgebildet ist und gegenüber der Gate-Elektrode durch einen Isolationsfilm getrennt ist, um einen Kondensator zu bilden; und

daß eine Diode (D1) zwischen der Source des ersten MOS-Transistors (Q1) und der Bitleitung ausgebildet ist und daß die Steuereinrichtung die Daten liest, indem sie das Potential auf der Wortleitung steuert, um ein Leiten oder ein Nichtleiten des zweiten MOS-Transistors in Abhängigkeit von der elektrischen Ladung zu verursachen, die in der Ladungsspeicherelektrode gespeichert ist, wodurch ein Ausgang auf der Bitleitung, die mit dem zweiten MOS-Transistor verbunden ist, erzeugt wird, der in Abhängigkeit von der Leitung oder der Nichtleitung des zweiten MOS-Transistors differiert.  
55

2. Einrichtung nach Anspruch 1, worin der Halbleiter Silizium ist.

transistor MOS formant une électrode de grille du second transistor MOS ;

le drain du second transistor étant connecté à une alimentation en énergie ;

la source du second transistor étant connectée à une ligne de bits, qui est soit la même que la première ligne de bits citée, soit séparée de celle-ci ;

5 ledit dispositif de mémoire comportant en outre un moyen de commande destiné à commander l'écriture de données dans la cellule de mémoire et la lecture de données à partir de cette cellule ;

ledit moyen de commande écrivant des données en commandant le potentiel sur la ligne de mots et la ligne de bits connectées au premier transistor MOS afin d'appliquer une charge électrique correspondant aux données sur la ligne de bits connectée au premier transistor MOS ;

10 ledit dispositif de mémoire à semiconducteurs étant caractérisé en ce que ladite électrode (28) d'emmaganage de charge est formée sur l'électrode de grille du premier transistor, étant séparée de l'électrode de grille par un film isolant pour former un condensateur ;

en ce qu'une diode (D1) est formée entre la source dudit premier transistor MOS (Q1) et la ligne de bits, et en ce que ledit moyen de commande lit des données en commandant le potentiel sur la ligne de mots pour provoquer une conduction ou une non-conduction du second transistor MOS suivant la charge électrique emmagasinée sur l'électrode d'emmaganage de charge, produisant ainsi un signal de sortie sur la ligne de bits connectée au second transistor MOS, le signal de sortie différant suivant la conduction ou la non-conduction du second transistor MOS.

2. Dispositif selon la revendication 1, dans lequel le semiconducteur est du silicium.

20 3. Dispositif selon la revendication 2, dans lequel la couche semiconductrice est une couche de silicium polycristallin.

4. Dispositif selon la revendication 1, dans lequel la source du premier transistor MOS est connectée à la ligne de bits pour l'écriture, et la source du second transistor MOS est connectée à une seconde ligne de bits pour la lecture, séparée de la ligne de bits mentionnée ci-dessus.

25 5. Dispositif selon la revendication 4, dans lequel une diode à jonction pn ou une diode de Schottky est formée entre le drain du premier transistor MOS et l'électrode d'emmaganage de charge.

6. Dispositif selon la revendication 5, dans lequel l'électrode d'emmaganage de charge est d'un type de conductivité différent du type de conductivité du drain du premier transistor MOS, pour qu'une diode à jonction pn soit formée entre eux.

30 7. Dispositif selon la revendication 5, dans lequel l'électrode d'emmaganage de charge est en métal pour former une diode à jonction Schottky entre elle et le drain du premier transistor MOS.

8. Dispositif selon l'une quelconque des revendications précédentes, dans lequel :

35 ledit moyen de commande applique un premier potentiel à la ligne de mots pour rendre conducteur le premier transistor MOS afin d'écrire des données, appliquant un premier potentiel à la source du premier transistor MOS pour écrire une donnée "1", et appliquant un second potentiel à la source du premier transistor MOS pour écrire une donnée "0" ;

ledit moyen de commande applique un deuxième potentiel à la ligne de mots pour maintenir le premier transistor non conducteur afin de retenir la donnée emmagasinée sur l'électrode d'emmaganage de charge ; et

40 ledit moyen de commande applique un troisième potentiel à la ligne de mots pour lire une donnée, afin de changer le potentiel sur l'électrode d'emmaganage de charge pour rendre le second transistor MOS conducteur ou non-conducteur suivant la donnée emmagasinée sur l'électrode d'emmaganage de charge, de manière à transmettre ou à ne pas transmettre le potentiel de l'alimentation en énergie à la source du second transistor MOS et donc à la ligne de bits qui lui est connectée, la transmission et la non-transmission du potentiel provenant de l'alimentation en énergie produisant des potentiels différents sur la ligne de bits connectée à la source du second transistor.

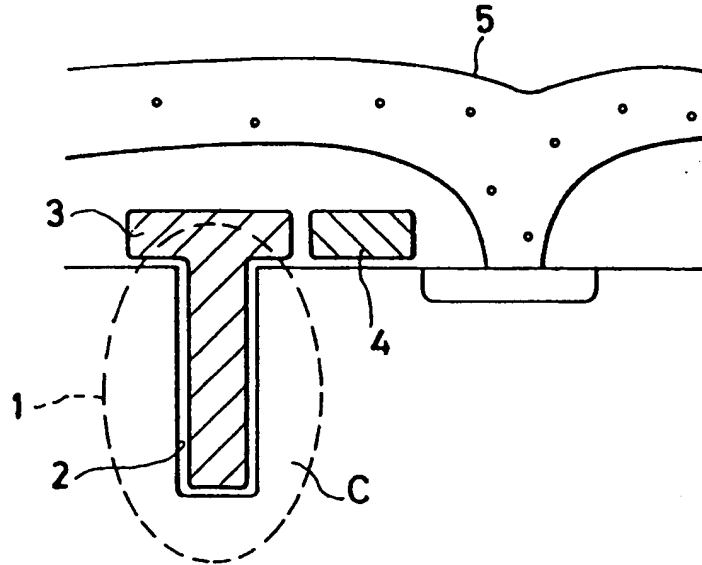
9. Dispositif selon la revendication 8, dans lequel le premier transistor MOS est un transistor à canal n, et le second transistor MOS est un transistor à canal p, et le troisième potentiel, tel qu'appliqué à la ligne de mots, est inférieur au deuxième potentiel tel qu'appliqué à la ligne de mots, lequel, lui-même, est inférieur au premier potentiel tel qu'appliqué à la ligne de mots, et le deuxième potentiel tel qu'appliqué à la source du premier transistor MOS est inférieur au premier potentiel tel qu'appliqué à la source du second transistor MOS.

10. Dispositif selon la revendication 8, dans lequel la source du premier transistor MOS et la source du second transistor MOS sont en contact l'une avec l'autre pour former une diode à jonction pn, et la source du second transistor est connectée à la ligne de bits commune utilisée à la fois pour l'écriture et la lecture.

55 11. Dispositif selon la revendication 8, dans lequel la source du premier transistor MOS et la source du second transistor MOS sont en contact l'une avec l'autre par l'intermédiaire d'une couche métallique pour former une diode à jonction Schottky pn entre la couche métallique et une première des sources, et la source du second transistor est connectée à la ligne de bits commune utilisée à la fois pour l'écriture et la lecture.

# FIG. 1

PRIOR ART



# FIG. 2

PRIOR ART

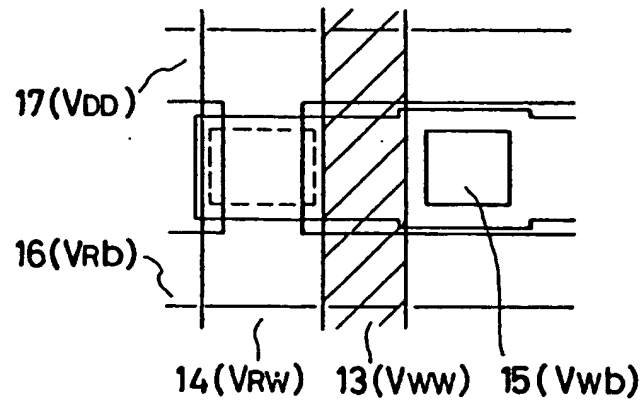


FIG. 5

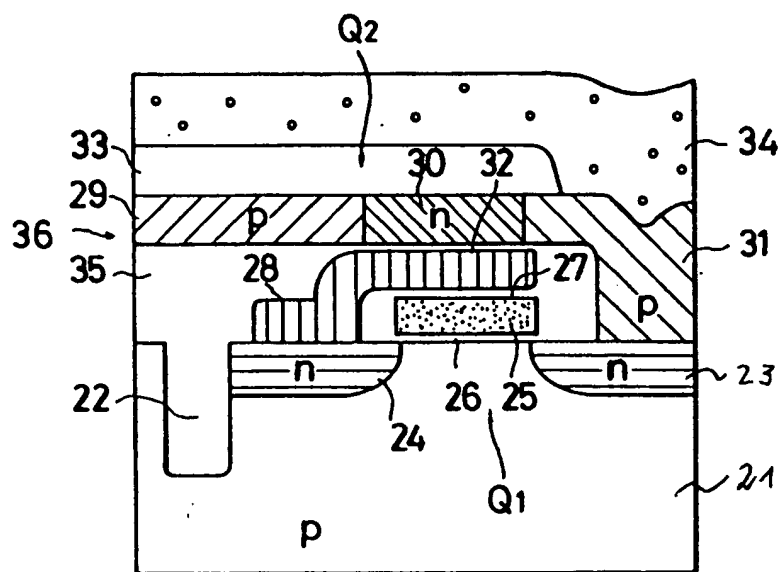


FIG. 7

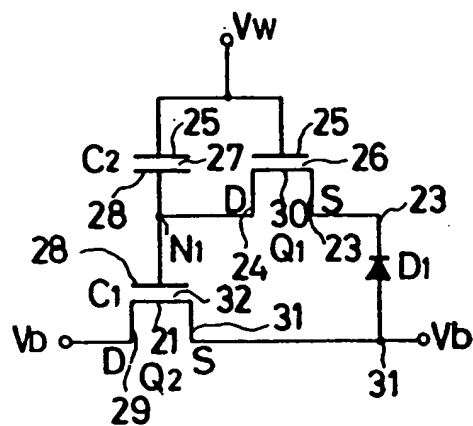


FIG.8a

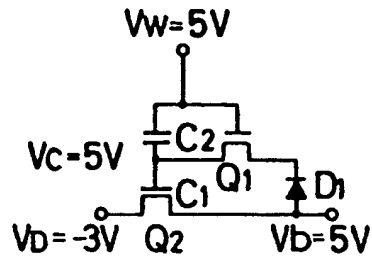


FIG.8b

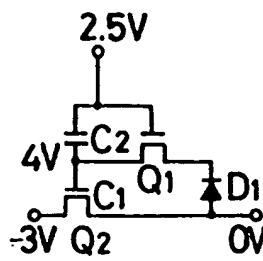


FIG.8c

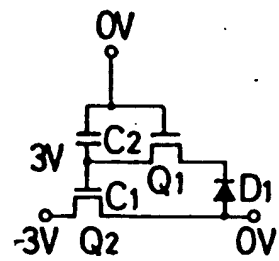


FIG.8d

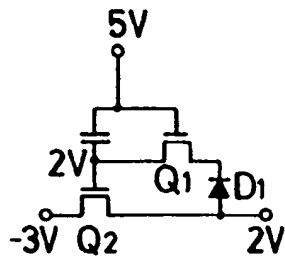


FIG.8e

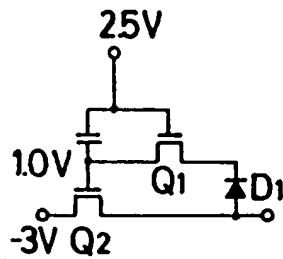


FIG.8f

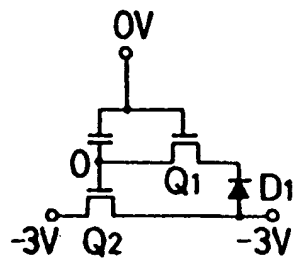


FIG.9

		Vw	Vb
WRITING	1	5 (V)	5(V)
	0	5	2
MAINTAINING		25	—
READING	1	0	0
	0	0	-3

FIG.11

